

**Amendments to the Claims:**

This listing of claims replaces all prior versions, and listings, of claims in this application.

**Listing of Claims:**

1. (Original) A digital spread spectrum frequency synthesizer, comprising:

a divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period;

a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider so that said divider generates said output clock by means of dividing said reference clock by said time-varying value;

means for adjusting said period control word by a period offset in response to said output clock; and

a filter for substantially filtering out jitter from said output clock.

2. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 1,

wherein said period control word has a bit resolution greater than that of said time-varying value.

3. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 1,

wherein said noise-shaped quantizer is a delta-sigma quantizer.

4. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 1,

wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output clock.

5. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 1, wherein said means for adjusting said period control word comprises:

an offset generator for generating said period offset in response to said output clock; and  
an adder for generating said adjusted period control word by means of adding said period offset to said a period nominal.

6. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 5, wherein said offset generator is an up/down counter.

7. (Currently amended) A digital spread spectrum frequency synthesizer, comprising:  
a noise-shaped quantizer for quantizing a period control word to a time-varying value;  
a divider for generating an output signal by means of dividing a reference signal by said time-varying value, said output signal feeding back to said noise-shaped quantizer so that said noise-shaped quantizer generates said time-varying value in response to said feedback output signal; and

means for adjusting said period control word by a period offset in response to said output signal clock.

8. (Currently amended) The digital spread spectrum frequency synthesizer as claimed in claim 7, further comprising a filter for ~~ef~~ significantly filtering out jitter from said output signal.

9. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output signal.

10. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said reference signal is a reference clock with a substantially fixed period.

11. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said output signal is an output clock with a time-varying period and a substantially precise long-term average frequency.

12. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said period control word has a bit resolution greater than that of said time-varying value.

13. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said noise-shaped quantizer is a delta-sigma quantizer.

14. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 7, wherein said means for adjusting said period control word comprises:  
an offset generator for generating said period offset in response to said output clock; and  
an adder for generating said adjusted period control word by means of adding said period offset to said a period nominal.

Serial No. 10/615,845  
Art Unit: 2611  
Inventor: Sterling SMITH et al.

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15. (Original) The digital spread spectrum frequency synthesizer as claimed in claim 14  
wherein said offset generator is an up/down counter.